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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/172,553	GREEN ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *1-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,4* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Drawings

➢ The drawings are objected to by the Draftsperson under 37 CFR 1.84. Applicant is required to submit a proposed drawing correction in reply to this Office Action.

Claim Rejections - 35 USC § 112

➢ The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

➢ Claims 16-18, 21-23, and 26-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites the limitation "storage poly". It is not clear to the Examiner whether the "storage poly" is a layer or a structure comprised of polysilicon.

Claim 17 recites the limitation "desired position" in line 15. It is not clear to the Examiner the meaning of the term "desired position."

Claim 17 recites the limitation " the storage poly " in line 17. There is insufficient antecedent basis for this limitation in the claim.

Claim 18 recites the limitation "storage poly." It is not clear to the Examiner whether the "storage poly" is a layer or a structure comprised of polysilicon.

Claim 18 recites the limitation "desired areas" in line 25. It is not clear to the Examiner the meaning of the term "desired areas."

Claim 21 recites the limitation "storage poly". It is not clear to the Examiner whether the "storage poly" is a layer or a structure comprised of polysilicon.

Claim 22 recites the limitation "desired position" in line 23. It is not clear to the Examiner the meaning of the term "desired position."

Claim 22 recites the limitation " the storage poly " in line 25. There is insufficient antecedent basis for this limitation in the claim.

Claim 23 recites the limitation "storage poly." It is not clear to the Examiner whether the "storage poly" is a layer or a structure comprised of polysilicon.

Claim 23 recites the limitation "desired areas" in line 5. It is not clear to the Examiner the meaning of the term "desired areas."

Claim 26 recites the limitation "storage poly". It is not clear to the Examiner whether the "storage poly" is a layer or a structure comprised of polysilicon.

Claim 27 recites the limitation " the storage poly layer " in line 10. There is insufficient antecedent basis for this limitation in the claim.

Claim 27 recites the limitation " the storage poly " in line 14. There is insufficient antecedent basis for this limitation in the claim.

Claim 28 recites the limitation "desired areas". It is not clear to the Examiner the meaning of the term "desired areas."

Claim 28 recites the limitation "storage poly". It is not clear to the Examiner whether the "storage poly" is a layer or a structure comprised of polysilicon.

Claim Rejections - 35 USC § 102

➢ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

➢ Claims 16, 21, 26, and 31-34 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Jost et al. (US Patent No. 5,686,747).

Regarding claim 16, Jost et al. teach a semiconductor memory device comprised of: a layer (**36**) which comprises a storage poly and a hemispherical-grain polysilicon layer (column 4, lines 42-46); and an upper surface (**30**) which is formed by masking and etching the layer (**36**) (column 4, lines 56-57).

Regarding claim 21, Jost et al. teach a semiconductor memory device comprised of: a layer (**36**) which comprises a storage poly and a hemispherical-grain polysilicon layer (column 4, lines 42-46); an upper surface (**30**) which is formed by masking and etching the layer (**36**) (column 4, lines 56-57); a dielectric material (**38**) over said etched storage poly (**36**) (column 4, lines 61-62); and a cell poly (**40**) over said dielectric material (column 5, lines 14-15).

Regarding claim 26, Jost et al. teach a semiconductor memory device comprised of: a semiconductor substrate (**11**) having at least one field oxide (**19**), actives area (**22**, **24**, **26**), at least one transistor gate member (**14**,**12**) residing between the active regions (**22**, **24**, **26**) (Figure 1); a layer (**36**) which comprises a storage poly and a

hemispherical-grain polysilicon layer (column 4, lines 42-46); an upper surface (**30**) which is formed by masking and etching the layer (**36**) (column 4, lines 56-57); a dielectric material (**38**) over said etched storage poly (**36**) (column 4, lines 61-62); and a cell poly (**40**) over said dielectric material (column 5, lines 14-15).

Regarding claims 31-34, Jost et al. teach a capacitor storage poly comprised of a plurality of contiguous mesas or webs (**31**) (Figure 4).

Claim Rejections - 35 USC § 103

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

➢ This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102((e), f) or (g) prior art under 35 U.S.C. 103(a).

➢ Claims 16-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jost et al. (US Patent No. 5,686,747) in view of Watanabe et al. (US Patent No. 5,623,243).

➢ Jost et al., as stated supra, essentially discloses the claimed invention but fails to show the steps of: etching the storage poly prior etching the hemispherical-grain polysilicon and planarizing the polysilicon layer to form the storage poly.

Regarding claims 17, 22, and 27, Watanabe et al. teach etching and patterning the storage poly using a resist (**7**) (figures 10c-10d).

Regarding claims 18-20, 23-25, and 28-30, Watanabe et al. teach a buffer layer (**2**) over a substrate (**1**), etching the buffer layer (**2**) using a resist (**3**) (Figure 10b); depositing and patterning polysilicon layers (**4**, **6**) to form the storage poly (Figure 10d).

➢ Regarding claims 16-34; a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17**. See also in re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear.

"Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the

claim is unpatentable even though the prior product is made by a different process." In re Thorpe, **227 USPQ 964, 966** (Fed. Cir. 1985).

➢ Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Jost et al. to include etching the storage poly prior etching the hemispherical-grain polysilicon and planarizing the polysilicon layer to form the storage poly since such modification would result in a semiconductor device having a large effective surface area, as described in Abstract of Watanabe et al.

Conclusion

➢ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Brown (US Patent No. 5,608,247) discloses storage capacitor structures using CVD TiN on hemispherical grain silicon. Harshfield (US Patent No. 5,612,558) discloses hemispherical grained silicon on refractory metal nitride. Thakur et al. (US Patent No. 5,658,381) disclose a method to form HSG silicon by implant seeding followed by vacuum anneal. Sun (US Patent No. 5,886,375) discloses a SRAM having improved soft-error immunity. Aiso et al. (US Patent No. 5,959,326) disclose a capacitor incorporated in semiconductor device having a lower electrode composed of multi-layers or of graded impurity concentration. Liu et al. (US Patent No. 5,170,233) disclose a method for increasing capacitive surface area of a conductive material in semiconductor processing and stacked memory cell capacitor. Batra et al. (US Patent No. 6,060,355) disclose a process for improving roughness of conductive layer. Okada

et al. (US Patent No. 6,066,872) disclose a highly reliable semiconductor device formed by solid phase growth at low temperature.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mahshid Saadat can be reached on (703) 308-4915. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
June 27, 2000

DAVID HARDY
PRIMARY EXAMINER